Time dependence of organic polymer thin-film transistors current

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ABSTRACT

We present results on the electrical characterization of gate-planarized organic polymer thin-film transistors (OP-TFTs). We investigated the time dependence of the OP-TFT current. Over a relatively short time range (several 100ms), we observed a decrease of the OP-TFT current corresponding to the establishment of the steady-state regime, and is slower when the transistor is in the weak accumulation regime or in the OFF-state. We believe that this is associated with carrier thermalization in the organic semiconductor. Over longer time scales, the decrease of the OP-TFT current is due to device aging and can be associated with a threshold voltage shift, up to 20V after an electrical stress at V_{GS}=–30V for 30min at room temperature. This shift is fully reversible once the gate polarization is removed and might be associated with charge trapping in the semiconductor.

Keywords: thin-film transistors, organic polymers, bias temperature stress, electrical instabilities, transient regime.

1. INTRODUCTION

Organic semiconductors can be divided into two main groups: oligomers and polymers [1,2]. In general, oligomers deposited by evaporation in vacuum have a highly ordered molecular structure while most of the time, organic polymers (OP) deposited by spin coating or inkjet printing over large areas at low temperature [3] are amorphous. Hence organic polymer thin-film transistors (OP-TFTs) usually show lower electrical performances than oligomer-based devices [1] but often exhibit better stability in air and lower OFF-current. Both types of organic materials have a considerable potential in large-area, low-cost, flexible organic electronics. They can be deposited on flexible, light-weight polymeric substrates instead of conventional glass [4] and, in combination with the organic polymer light-emitting diodes (OP-LED), these devices could be used to make very attractive all-organic polymer flexible display systems [5].So far, many research groups have been using device test structures, in which no patterning of organic and inorganic (especially gate electrode and insulator) layers is involved. State-of-the art field-effect mobility values reported for organic polymer TFTs with patterned gate electrode are typically in the range of 10^{-3} to 10^{-1}cm^2/Vs [6].

2. OP-TFTS USED IN THIS STUDY

1. Device structure

The device structure used in this study is an inverted staggered, gate-planarized TFT with bottom source / drain contacts fabricated on c-Si substrates covered with 1µm-thick silicon dioxide. A schematic cross-section of the device is shown in Figure 1. The plate fabrication steps are as follows. First, the 800Å-thick Cr gate electrode was sputtered and patterned. The gate electrode was then planarized using 2500Å of spin-coated benzocyclobutene (BCB), to achieve a mostly flat surface. A 1000Å-thick gate insulator layer, amorphous silicon nitride (a-SiN_x:H), was deposited by plasma-enhanced chemical vapor deposition (PECVD). The resulting total gate insulator capacitance per unit area is C_{ins}=7.5×10^{-9}F/cm^2. A 1700Å-thick indium-tin oxide (ITO) layer was sputtered, annealed and patterned to form the source and drain (S/D) contact electrodes. Finally, the organic polymer layer (1000 to 2000Å-thick) was spin-coated on the sample and the device was annealed in a vacuum oven (1hour at 90°C). We chose to deposit the organic material after the fabrication of the source and drain electrodes to avoid any risk of degradation of the organic layer due to subsequent processing steps. The organic semiconductor layer is a spin coated film fabricated from a solution of F8T2

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(poly-9,9-dioctylfluorene-co-bithiophene) in xylenes. The typical channel lengths and widths of our devices are 6-96μm and 56-116μm, respectively.

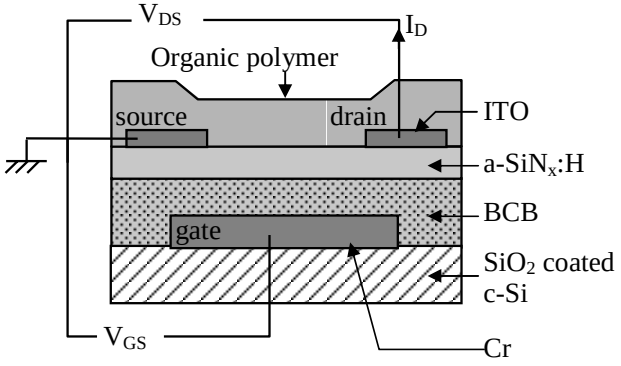


Figure 1: Schematic cross-section of our gate-planarized OP-TFTs.

2. Standard characterization methods

We used a Karl Suss PM8 probe station, HP 4156A semiconductor parameter analyzer and Interactive Characterization Software (ICS, by Metrics Technology Inc, Albuquerque, NM). The electrical characteristics of our devices were measured in the air, at room temperature and in the dark, unless specified otherwise. When we measure the OP-TFT transfer characteristics (I_D-V_{GS}), the gate voltage is set to its initial value and after waiting for a certain time (hold time), the gate voltage sweep begins. Each voltage step is followed by a delay time before the TFT drain current is actually measured. We usually start the transfer characteristic measurement in the TFT ON-state, then sweep the gate voltage towards the TFT OFF-state. This measurement method ensures that the TFT is in the steady-state regime throughout most of the transfer characteristics measurement. The TFT output characteristics (I_D-V_{DS}) measurement procedure is not as critical because the TFT accumulation state does not change throughout the measurement (V_{GS} is constant) but consistent procedures are used nevertheless [7].

Although the exact theory of OP-TFT operation is still under investigation, the MOSFET theory as modified for amorphous semiconductor based TFTs provides a good description of the device behavior. Consequently, we extract the TFT field-effect mobility and threshold voltage in the linear regime at low source-drain voltage from the following equation:

$$I_{DS} = -\mu_{FE\ lin} C_{ins} \frac{W}{L} \left(V_{GS} - V_{T\ lin}\right) V_{DS} \tag{1}$$

In the saturation regime, we use:

$$I_{DS} = -\mu_{FE\ sat} C_{ins} \frac{W}{2L} \left(V_{GS} - V_{T\ sat}\right)^2 \tag{2}$$

We should note that OP-TFTs do not always follow perfectly the MOSFET equations (1) and (2). It is often necessary to include the gate voltage dependence of the field-effect mobility by using an additional parameter γ [8] and modifying the equations for the linear and saturation regimes as follows:

$$I_{DS} = -\mu_{FE\ lin} C_{ins} \frac{W}{L} \left(V_{GS} - V_{T\ lin}\right)^{\gamma} V_{DS} \tag{3}$$

and

$$I_{DS} = -\mu_{FE\ sat} C_{ins} \frac{W}{(\gamma+1)L} \left(V_{GS} - V_{T\ sat}\right)^{\gamma+1} \tag{4}$$

The parameter γ has been associated, in inorganic amorphous semiconductor devices, with the density of states in the semiconductor, but further analysis is needed in the case of organic semiconductor devices.

The OP-TFT subthreshold swing S is extracted from [9]

$$I_{DS} \propto 10^{-V_{GS}/S} \tag{5}$$

3. Typical electrical performance of our OP-TFTs

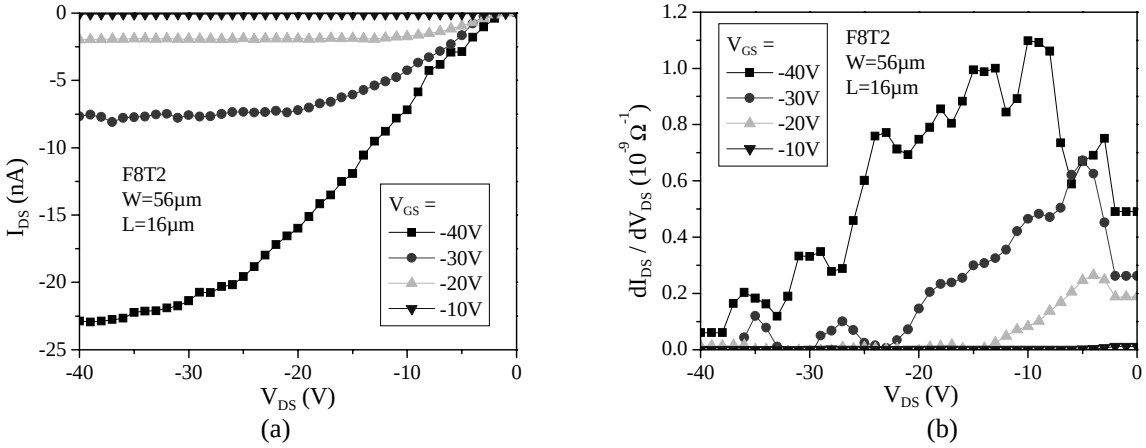


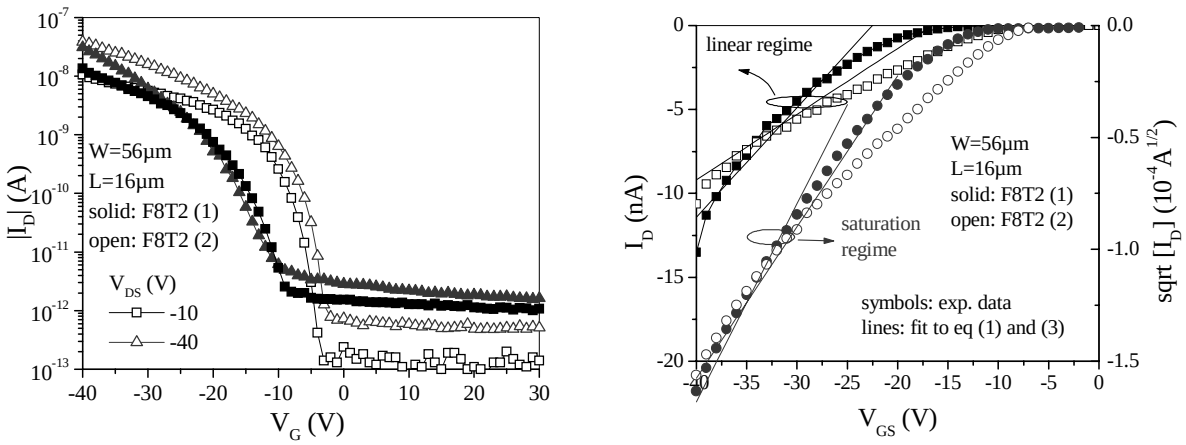
Figure 2: (a) Typical output characteristics for F8T2 based OP-TFT. (b) Derivatives of the curves in (a).

Typical OP-TFT output (drain current versus drain voltage, I_D-V_{DS}) characteristics and their derivatives are plotted in Figure 2(a) and (b), respectively. We can see that saturation of the current is observed for large source-drain voltages and that the curves exhibit a small amount of current crowding near the origin. This non ideality, also clearly observed in Figure 2(b), is usually associated with non-ideal source and drain contacts.

Transfer characteristics in the linear and saturation regimes for the same devices as in Figure 2 are shown in Figure 3. Lines in Figure 3(b) correspond to the fits to equations (1) and (2) used to extract the field-effect mobility and threshold voltage; lines in Figure 3(a) correspond to the fit to equation (5), used to calculate the subthreshold swing. We can clearly see that, although the standard MOSFET model provides an acceptable initial description of the OP-TFT behavior, it is not ideal [8]. The electrical parameters obtained for a typical OP-TFT are summarized in Table 1. We should note that, as we observed in most cases, the field-effect mobility extracted in the saturation regime is slightly higher than the field-effect mobility extracted in the linear regime. To compare the performance of devices with different geometry, gate insulator characteristics or measurement conditions, some of the OP-TFT electrical parameters had to be normalized. More specifically, we believe that the equivalent charge or normalized threshold voltage ($V_T \times C_{ins}$) should be used. In addition, from the value of the subthreshold slope, we can also calculate the equivalent maximum density-of-states that can be present at the organic layer/gate insulator interface:

$$N_{ss}^{max} = \left(\frac{S \log(e)}{kT/q} - 1 \right) \frac{C_{ins}}{q} \qquad (6)$$

where q is the electron charge, k the Boltzmann constant and T the temperature.



(a) (b)

Figure 3: Typical transfer characteristics of our OP-TFTs in linear and saturation regimes.

Table 1: Typical electrical parameters of our OP-TFTs

W/L	56/16
Ci (F/cm^2)	7.5×10^{-9}
$\mu_{FE\ lin}$ (cm^2/Vs)	1.5×10^{-3}
$V_{T\ lin}$ (V)	-16.5
$V_{T\ lin\ norm}$ (C/cm^2)	-1.2×10^{-7}
$\mu_{FE\ sat}$ (cm^2/Vs)	3.5×10^{-3}
$V_{T\ sat}$ (V)	-16.5
$V_{T\ sat\ norm}$ (C/cm^2)	-1.2×10^{-7}
S (V/dec)	1.5
$N_{ss}^{max} = \left(\frac{S\log(e)}{kT/q} - 1\right)\frac{C_i}{q}$ (cm^{-2}eV^{-1})	1.2×10^{12}
ON/OFF ratio (in linear regime)	10^5

3. RESULTS AND ANALYSIS

Our experiments were based on the measurement of the time dependence of the OP-TFT current while constant voltages are applied on the source, gate and drain. We initially performed these experiments for a relatively short time, i.e. typically a few seconds. A constant source-drain voltage was used (-10V) and the OP-TFT current was measured for different gate voltages between 0 and -40V. The resulting data is plotted in Figure 4, we can see that the magnitude of the current initially decreases with time, then reaches a constant value. On a short time scale, this change of the TFT current is associated with the time needed for the device to reach the steady-state regime. It is a relatively slow process and takes significantly more time (several seconds) when the TFT is in weak accumulation or in the OFF-state, as seen in Figure 4. We should note that, when the OP-TFT is in the OFF state (V_{GS}=0V), the current reaches the measurement accuracy limits (a few 0.1pA) before the steady state regime seems to be established. More precisely, transient phenomena can be associated with carrier thermalization, i.e. trapping and detrapping of carriers in the deep-gap defect states [10]. This process is faster in regions where the density of accumulated carriers is high. In amorphous inorganic semiconductors such as a-Si:H, thermalization after gate voltage switch on occurs faster near the gate insulator /

semiconductor interface and is followed by movement of charges away from the interface towards the bulk of the semiconductor [10]. Further analysis is required for organic semiconductors, but we believe that the processes following gate voltage switch ON and OFF can be analyzed using a similar concept. The thermalization phenomenon would explain why the transient current decay occurs on a very small time frame in the OP-TFT ON-state (typically V_{GS}=-40V), because of the large concentration of accumulated carriers in the channel. On the other hand, in the OFF-state (typically V_{GS}=0V), the concentration of accumulated carriers is lower and the thermalization is consequently much slower, resulting in a longer current decay, as shown in Figure 4.

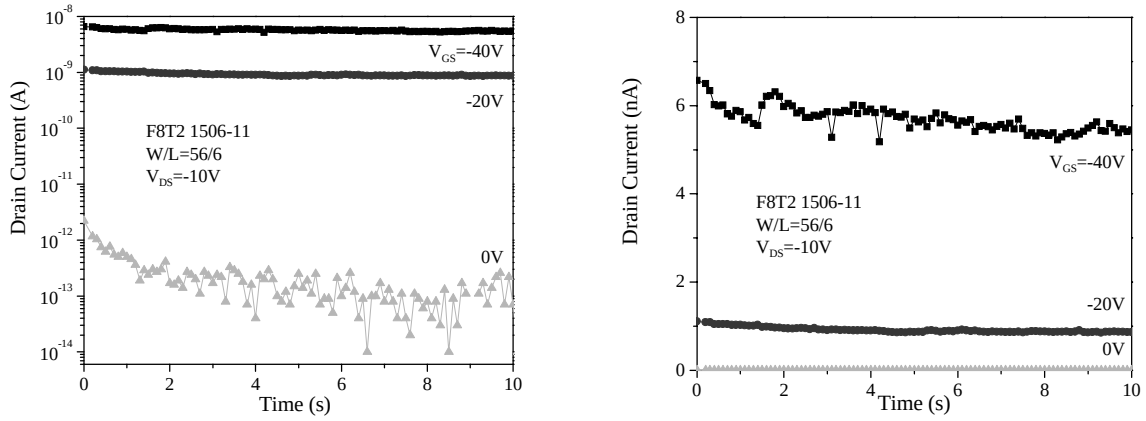


Figure 4: Time evolution of the TFT current on a short time scale.

On a longer time scale, the magnitude of the TFT current continues to decrease and the change in current is even more significant as seen in Figure 6. This current decrease is due to the device electrical instabilities. Measurements of the TFT transfer characteristics before and after the experiment clearly show a shift in threshold voltage, as seen in Figure 5. The measurement of the time dependence of the TFT current over a long time scale acts as an electrical stress experiment. We should note that, after the bias stress is removed, the device relaxes towards its initial state, as shown in Figure 5. This relaxation is relatively fast, even at room temperature and is accelerated by illumination. This is consistent with a recently published study [11], but further experiments are needed to accurately described this relaxation phenomenon in our devices.

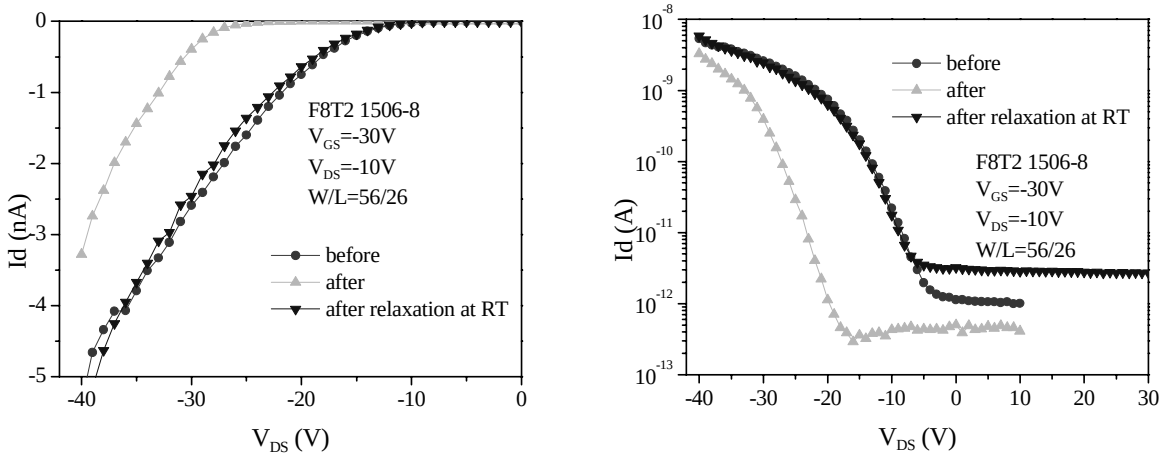


Figure 5: OP-TFT transfer characteristics before and after long-time scale measurement.

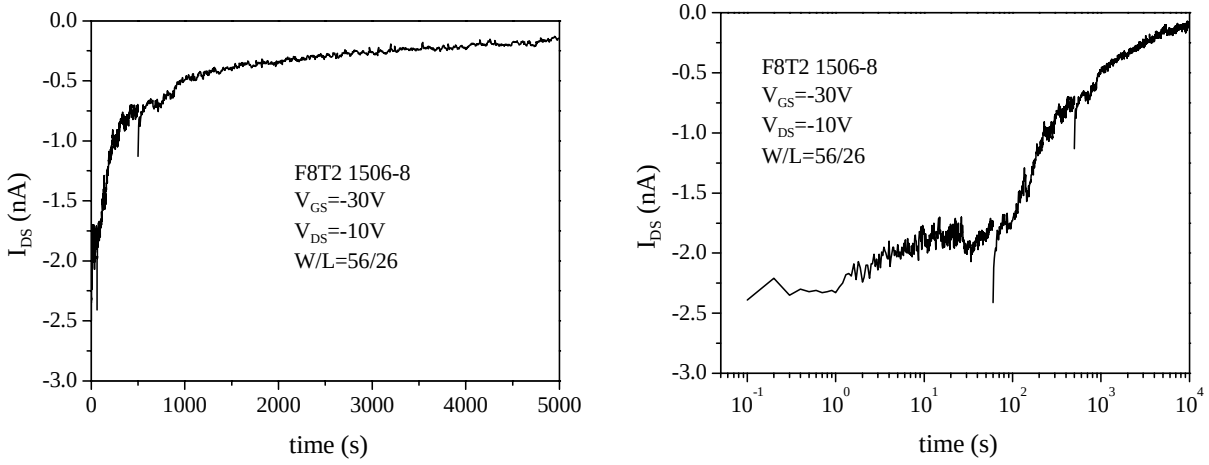


Figure 6: Time evolution of the TFT current on a long time scale.

Conventional bias temperature stress (BTS) experiments have also been performed, in which the device is subjected to a constant (DC) gate bias during a given stress time, at a given stress temperature. At several pre-selected times, the stress is interrupted and a transfer characteristic is measured before resuming the electrical stress. Transfer characteristics obtained during such a stress, for conditions identical to the ones used in the experiments corresponding to Figure 4 and Figure 6 are shown in Figure 7.

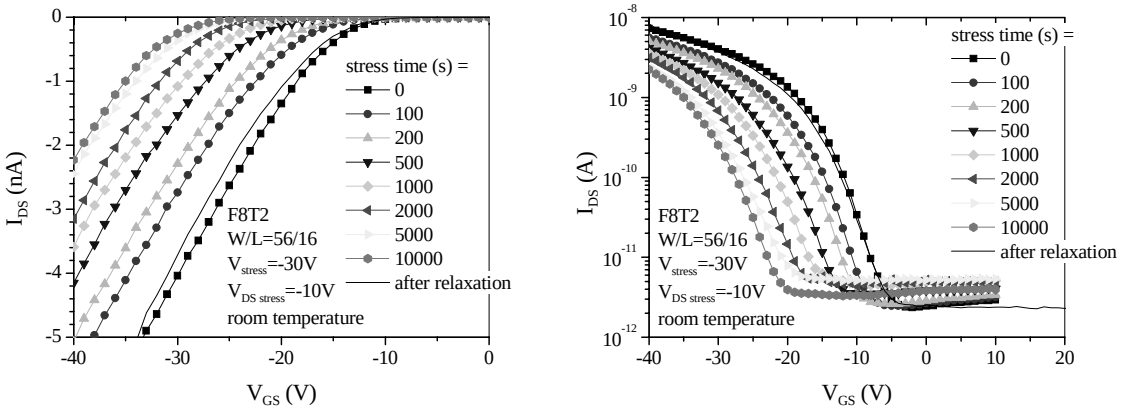


Figure 7: Transfer characteristics after bias stress experiments of different durations.

We have verified that comparable threshold voltage shifts were obtained after both experiments, as shown in Figure 8.

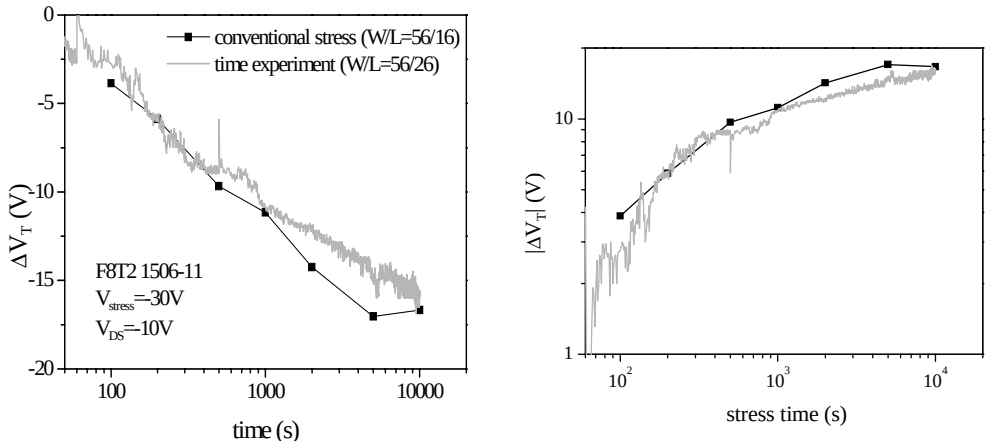


Figure 8: Threshold voltage shifts extracted from the time experiment and the conventional bias stress experiment.

We have also investigated the dependence of the threshold voltage shift obtained after bias temperature stress on the stress parameters, i.e. stress time, stress voltage and stress temperature. We have observed that the threshold voltage shift versus stress time curves can be fit by the following stretched exponential equation, based on the analysis developed for a-Si:H TFTs [12]:

$$\Delta V_T = B\left(1-\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right) \tag{7}$$

where B, β and τ are fitting parameters that can depend on the stress voltage and stress temperature. Figure 9(a) and Figure 10(a) show our experimental data for different BTS conditions and the corresponding fits to equation (7). We can see that we have obtained very acceptable fits using this equation.

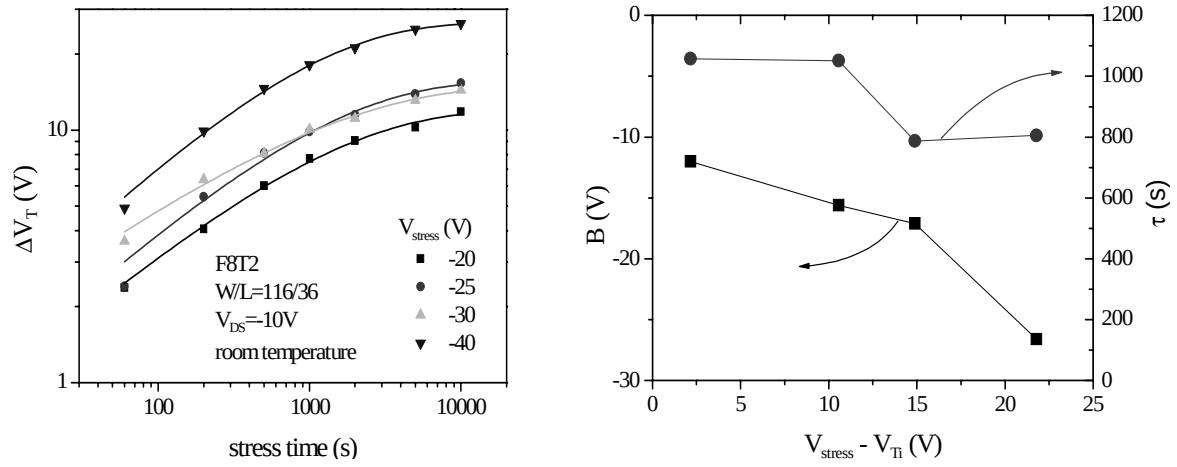


Figure 9: (a) Threshold voltage shift at different stress voltages and constant stress temperature. Symbols show experimental data, lines show fit to the stretched exponential equation. (b) Variations of B and τ fitting parameters used in (a) with the stress voltage above the initial threshold voltage.

We have also investigated the effect of the stress voltage and stress temperature on the three fitting parameters. We have observed that B increases with the stress voltage, approximately showing a roughly linear dependence with V_{stress}-V_{Ti}. Its

dependence with the stress temperature seems to be mostly associated with the temperature effect on the initial threshold voltage. The parameter β is roughly independent of the stress voltage and increases with the stress temperature. The parameter τ decreases with both stress voltage and stress temperature. However, further BTS experiments are needed to describe more accurately the exact variations of these parameters.

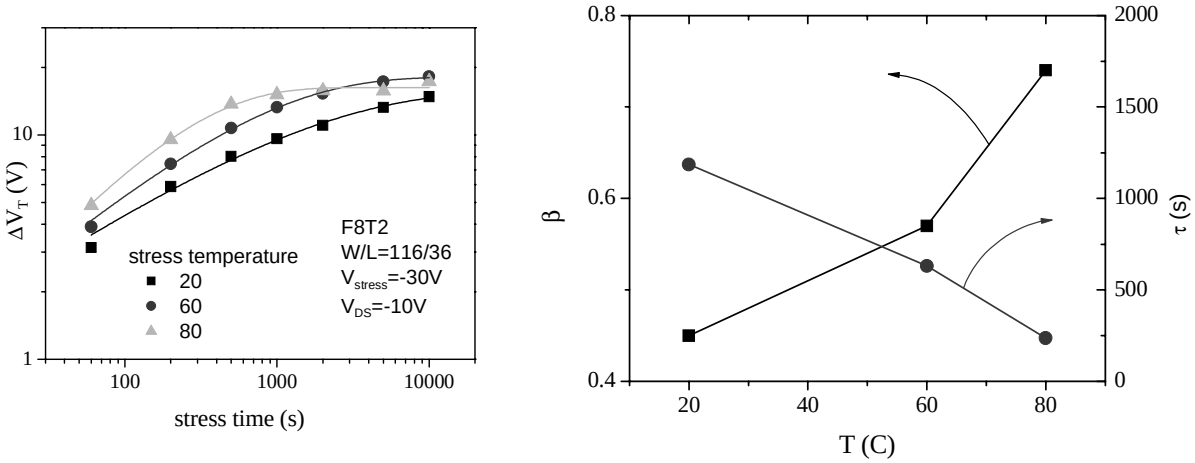


Figure 10: (a) Threshold voltage shift at different stress temperature and constant stress voltage. Symbols show experimental data, lines show fit to the stretched exponential equation. (b) Variations of β and τ fitting parameters used in (a) with the stress temperature.

CONCLUSION

We have investigated the transient currents observed in our gate-planarized organic polymer TFTs. We have described the short term transient currents using a carrier thermalization concept, initially developed for inorganic amorphous semiconductor devices, which explains the gate voltage dependence of the current decay. For longer time scales, the transient currents observed in our devices are clearly associated with device aging, and more precisely with a threshold voltage shift. Further analysis of the electrical instabilities of the OP-TFTs has been performed and we have presented the influence of the stress parameters, i.e. time, voltage and temperature, on the threshold voltage shift.

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